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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/988,126	11/19/2001	Jeong Won Heo	HEOJ3002/REF	8171

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EXAMINER	
MURPHY, RHONDA L	
ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 05/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/988,126	Applicant(s) HEO ET AL.	
	Examiner Rhonda Murphy	Art Unit 2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9 and 14* is/are rejected.

7)☒ Claim(s) *6-8,10-13 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/14/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority under 35 U.S.C. 119(a)-(d). The certified copy has been filed in parent Application No. PCT/KROO/00494, filed on May 19, 2000.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 4, 5, 9 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wicklund (US 6,295,295) in view of Yasukawa et al. (US 2005/0083939).

Regarding claim 1, Wicklund teaches a switch fabric comprising: a first registering means for temporarily storing an input cell (Fig. 2, port 8; col. 5, line 50); a second registering means for storing VCI values for a plurality of cells including the input cell provided from the first registering means (header table 16, col. 5, lines 51-54) and outputting each of the VCI values after a predetermined cell time (since the VCI values are stored temporarily, the VCI values will be outputted after a certain period of time); and logical queuing means for sorting the cells based on their VCI values to thereby place each of the cells at a proper position in a corresponding logical queue (Fig. 3,

scheduler 18; col. 6, lines 30-34) and outputting each of the cells in response to the outputted VCI value (since the queuing means is a temporary storage, the cells will be subsequently outputted).

Wicklund fails to explicitly teach sorting the cells based on their time stamp values. However, time stamping occurs to indicate the time in which a cell arrives at a specified location.

Yasukawa teaches logical queuing means for sorting the cells based on their time stamp values (page 12, paragraph 247).

Furthermore, the combined system of Yasukawa and Wicklund teach cells having a same VCI value arranged in one corresponding logical queue according to the order of their time stamp values.

In view of this, it would have been obvious to one having ordinary skill in the art, to incorporate the sorting of time stamp values into Wicklund's system, for the purpose of minimizing delay by outputting the cells with the earliest time stamp.

Regarding claim 2, the combined system of Wicklund and Yasukawa teach sorting and storing cells based on their VCI and time stamp values. Wicklund further teaches a buffering means for storing the cells in corresponding logical queues until the cells are outputted (Fig. 3, queue 40; col. 6, lines 12-14); a storage means for containing a VCI value corresponding to each of the logical queues (queue 50; col. 6, lines 30-38) and a buffer address representing a position of a head cell in each of the logical queues (col. 9, lines 20-24); and a controlling means for managing an input and output process of

the buffering means based on the VCI values of the cells (controller 31, col. 6, lines 5-11).

Wicklund fails to explicitly teach buffering means based on time stamp values of the cells.

However, Yasukawa teaches means for buffering the cells based on their time stamp values (page 12, paragraph 247).

In view of this, it would have been obvious to one having ordinary skill in the art, to incorporate the buffering means of time stamp values into Wicklund's system, for the purpose of minimizing delay by outputting the cells with the earliest time stamp.

Regarding claim 4, Wicklund further teaches a content addressable memory (CAM) for storing the VCI value corresponding to each of the logical queues (Fig. 3, queue 50; col. 6, lines 30-38); and random access memory (RAM) for storing the buffer address representing the position of the head cell in each of the logical queues (col. 6, lines 57-59).

Regarding claim 5, the combined system of Wicklund and Yasukawa teach sorting and storing cells based on their VCI and time stamp values. Wicklund further teaches a cell data field (CDF) for storing the cells (Fig. 3, Current queue 42; col. 6, lines 17-29); and a next address field (NAF) for storing addresses of successive cells in each of the logical queues (Next queue 41; col. 6, lines 17-29).

Wicklund fails to explicitly teach storing time stamp values of the cells. However, time stamping values are stored to indicate the time in which a cell arrives at a specified location.

Yasukawa teaches logical queuing means for storing the cells based on their time stamp values (page 12, paragraph 247).

In view of this, it would have been obvious to one having ordinary skill in the art, to incorporate the storing of time stamp values into Wicklund's system, for the purpose of recording the time at which a cell arrives in order to output the cell with the earliest time stamp.

Regarding claim 9, the combined system of Wicklund and Yasukawa teach sorting and storing cells based on their VCI and time stamp values. Wicklund further teaches a first field for storing the cells and extracting the cells by the controlling means (col. 5, lines 58-67) and a second field for storing the addresses of successive cells in each of the logical queues (col. 6, lines 19-29).

Wicklund fails to explicitly teach storing time stamp values of the cells. However, time stamping values are stored to indicate the time in which a cell arrives at a specified location.

Yasukawa teaches logical queuing means for storing the cells based on their time stamp values (page 12, paragraph 247).

In view of this, it would have been obvious to one having ordinary skill in the art, to incorporate the storing of time stamp values into Wicklund's system, for the purpose of recording the time at which a cell arrives in order to output the cell with the earliest time stamp.

Regarding claim 14, Wicklund teaches examining a VCI value of an input cell and transmitting the input cell to a logical queue that has a same VCI as that of the input cell

(col. 5, lines 50-52; col. 6, lines 30-34); placing the input cell at a proper position in the logical queue by comparing cells stored in the logical queue (col. 6, lines 30-34); repeating the above steps for a plurality of input cells (numerous cells are transmitted through the switch, hence the process will be repeated for each inputted cell); selecting a head cell among the cells stored in the logical queue by using the VCI value of the input cell as an index after a predetermined cell time (col. 7, lines 11-20); outputting the head cell as an output cell (col. 7, lines 17-18); and repeating the steps above steps for the remaining cells among the input cells (numerous cells are transmitted through the switch, hence the process will be repeated for each inputted cell).

Wicklund fails to teach a time stamp value of the input cells.

However, Yasukawa teaches logical queuing means for comparing cells based on their time stamp values (page 12, paragraph 247).

Furthermore, the combined system of Yasukawa and Wicklund teach cells having a same VCI value arranged in one corresponding logical queue according to the order of their time stamp values.

In view of this, it would have been obvious to one having ordinary skill in the art, to incorporate the comparison of time stamp values into Wicklund's system, for the purpose of minimizing delay by outputting the cells with the earliest time stamp.

3. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wicklund and Yasukawa as applied to claim 3 above, and further in view of Chao (US 5,381,407).

Regarding claim 3, the combined system of Wicklund and Yasukawa teach logical queuing means and buffering means.

Wicklund and Yasukawa fail to teach an idle address.

However, Chao teaches an idle address providing means for supplying an idle address of the buffering means to the controlling means upon arrival of the input cell, wherein an address of an outputted cell is transmitted to the idle address providing means and treated as the idle address (col. 7, lines 47-68).

In view of this, it would have been obvious to one having ordinary skill in the art, to combine the systems of Wicklund and Yasukawa with Chao's idle address, for the purpose of storing addresses of empty cells.

Allowable Subject Matter

4. Claims 6-8, 10-13 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

*Calvignac et al. (US 5,629,928) discloses a dynamic fair queuing to support best effort traffic in an ATM network.

*Heiman (US 6,735,203) discloses a switch arrangement.

*Kline et al. (US 5,812,527) discloses simplified calculation of cell transmission rates in a cell based network.

*Agnevik et al. (US 6,738,381) discloses an ATM time stamped queuing.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rhonda Murphy whose telephone number is (571) 272-3185. The examiner can normally be reached on Monday - Friday 8:00 - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi Pham can be reached on (571) 272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Rhonda Murphy
Examiner
Art Unit 2667

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CHI PHAM
SUPERVISORY PATENT EXAMINE
TECHNOLOGY CENTER

9/28/05